ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

COMPARATIVE STUDY OF DRAM AND MRAM (STT-MRAM)

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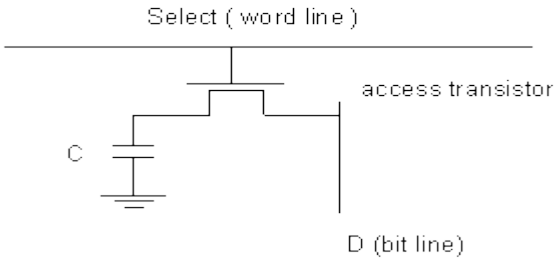
ABSTRACT

High memory latency and limited memory bandwidth have proven to be the biggest problems for the performance of computer system on various computer applications. To solve this problem designers have made an effort to increase the amount of on chip memory. Till now we have being using SRAM for various applications. But now-a-days alternate technologies like DRAM and STT-MRAM are progressing to enhance the on chip memory capacity at the same cost of higher latency. Various types of memory systems are developed using DRAM (1Tdram, e-dram) and MRAM (STT-MRAM, Thermal MRAM).The performance of each type of memories has been developed in the following paper. In this paper parameters like cell area, power and reliability have been considered. The most important parameter read and write time gives us a clear picture of throughput and latency of such memories systems. The conclusions of the paper tells us that both types of memories have advantage over the other in some or the other aspect. But if we compare these results with the existing SRAM results for the same parameters we come to know that these memory systems are more advantageous than SRAM. The results are very much helpful for design and verification with maintenance purposes.

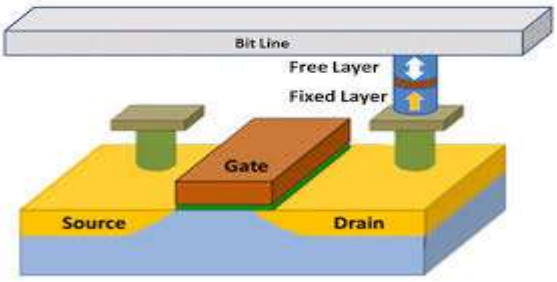
KEYWORDS— Power, Endurance, Read Write Time, Technology, Maturity, Cell size, Reliability.

INTRODUCTION

In dynamic RAM, a single memory cell is implemented using a single transistor and a capacitor which occupy lesser space as compared to six transistors which are used to implement a SRAM. The capacitor based memory is known as dynamic RAM (DRAM). Each elementary DRAM cell is made up of a single MOS transistor and a storage capacitor. Each storage cell contains one bit of information. This charge, however, leaks off the capacitor due to the sub-threshold current of the cell transistor. Therefore, the charge must be refreshed several times each second. The memory cell is written to by placing a "1" or "0" charge into the capacitor cell. This is done during a write cycle by opening the cell transistor (gate to power supply or VCC) and presenting either VCC or 0V (ground) at the capacitor. The word line (gate of the transistor) is then held at ground to isolate the capacitor charge. This capacitor will be accessed either for a new write, a read or a refresh. Magnetoresistive random access memory (MRAM) employs ferromagnetic storage devices integrated with semiconductor circuitry to provide a nonvolatile random access memory with fast read and write as well as virtually unlimited read and write cycles. Each MRAM bit contains a magnetic tunnel junction (MTJ) consisting of two ferromagnetic layers separated by a thin (~ 1 nm) insulating layer. Data is stored in terms of the magnetization direction of one of the ferro magnets (the free layer) either parallel or antiparallel to the other (the fixed layer). A tunnel magnetoresistance (MR) that is low (high) for parallel (antiparallel) magnetization provides the read-out signal.This document therefor analysis the characteristics of both DRAM and MRAM and helps to compare the features and scalability of MRAM memories to evolutionary DRAM technologies and to present preliminary results of their characteristics.



1T DRAM CELL



1T MRAM CELL

PERFORMANCE PARAMETERS:

Advances in fabrication technology have resulted in a number of memory technologies like embedded DRAM and MRAM. In this section various device level and operating characteristics of these technologies would be discussed. This qualitative and quantitative summary would help us to know advantages and disadvantages of both types of memories.

Device Level Characteristics-

These include parameters like maturity, cell area, power and reliability. These parameters are heavily influenced by the physical characteristics and type of fabrication process used.

1. Maturity

Maturity in new designs means whether the technology is currently used in market or it is in early or later research stages before being commercially mature. Now here as we know DRAM is a product and is commercially available for various applications [1]. But the case is not same for MRAM (STT-RAM), it is still developing and is in the advanced developed stage

2. Cell Area

The cell area plays an important role in determining the viability and application of the memory designed. Previously, DRAM was developed for having minimum cell area. The cell area can be represented by the process technology independent metric λ which is equal to half minimum feature size of the particular technology. The recent embedded DRAM designs have demonstrated 80λ2 cells [6]. In comparison to this several MRAM cell designs have been proposed with the area ranging from 12λ2 for the GMR MRAM to 6λ2 for TMR MRAM architecture. But demonstrated MRAM have areas up to 80λ2 [3].

3. Power

With shrinking sizes and increased transistor counts, power has become an important constraint. Dynamic power is increasing due to increasing clock rates while static power is increasing because of larger leakage currents resulting from lower threshold voltages. Power consumption is related to performance and complex designs consume more power and vice-versa. From results we come to know that DRAM consumes 10W power for 0.175µm fabrication technology. In case of MRAM initially demonstrated 24mW [2] power consumption for 0.6µm technology. To compare these results we divide the power consumption by the size and the frequency of the part to obtain the independent metric J/bit.

The summary table shows that power consumption of DRAMs is lower and it is potentially higher for MRAMs.

But in case of MRAMs the power may reduce as technology scales down and power/performance trade-offs are made [9]. For instance, DRAMs for lower power can be achieved by sacrificing the performance a bit. However MRAMs have to face the difficulty of unequal power requirements for write and read operations. A reference shows that write operation requires 8 times the read operation power.

4. Reliability
Integrated circuits are becoming noisier as sizes continue to decrease. Thus, reliability is becoming more important in memory designs. The reliability is directly proportional to the storing capacity of the memory. Now as per the existing knowledge DRAMs store information in the capacitor charge whereas MRAMs store information in the spin of electrons in the ferromagnetic material. Due to this MRAMs are less susceptible to strike from external energized materials compared to DRAMs [7]. But this makes it susceptible to stray magnetic fields to a small extent. Hence MRAMs are more reliable compared to DRAMs as they are nonvolatile has the data cannot be lost for a long period of time but in DRAMs as the charge of the capacitor decreases the data is lost.

Operational Characteristics:
The operational characteristics include parameters like read & write time, endurance, achievable bandwidth. These parameters depend mostly on architectural organization of the memory technology

1. Read and Write Times
The Read time is defined as the interval from where the address is placed on the address bus and when the data is available on the sense amplifiers. Read time is an important factor of the latency of a given memory system. For 0.18µm technology of DRAM 3.7ns was read time observed. MRAM time was almost 50ns for a 0.6µm fabrication technology used.

For DRAM architectural techniques like page mode access are used to reduce the access time latency. However, page mode access results in the first access to DRAM to be slower than the later accesses for the same row. This significantly affects the performance applications which have irregular memory accesses. DRAM needs to be refreshed and cannot be read during refreshing. This is one of the drawbacks of DRAM.

MRAM do not need to be refreshed and hence this limitation is eliminated.

Write times usually differ very much for DRAM and MRAM. Write time for MRAM do require more currents than reads and hence are slower [7]. However writes are not on critical path and hence architectural techniques like store buffers can be used to reduce latency.

2. Endurance
Endurance is a very basic parameter used to know the time for effective writing. In other words it means the number of write cycles that a memory cell endures before eventually wearing out. Now between these two memories i.e. DRAM and MRAM the endurance value is equal and is greater than 1015. But it is predicted that endurance of MRAM can be increased as the technology advances

3. Achievable Bandwidth
The achievable bandwidth for a memory depends on the architectural design of the system. Off chip DRAMs have been organized high latency high bandwidth devices. Recent studies show that DRAMs have 128Gbps throughput at 1GHz [1]. MRAMs have cell size similar to DRAMs can take advantage of vertical I/O pins. Hence, they are likely to have more bandwidth. However, MRAMs are in their preliminary stage and hence it is not clear how advantageous the vertical I/O pins will be in increasing the bandwidth.

PRELIMINARY ESTIMATES OF DRAM AND MRAM

Table 1:

	DRAM	MRAM
Technology	0.18µm	0.6µm
Maturity	Product	Advanced Development
Cell size	$80\lambda^2$	$12\lambda^2$ -$6\lambda^2$
Power	10W	24mW

Normalized Power (J/bit)	$1.2x10^{-15}$	$4.6x10^{-15}$
Read Time	3.7ns	50ns
Endurance	$>10^{15}$	$>10^{15}$
Bandwidth	128 Gbps	N.A
Non- Volatility	No	Yes

CONCLUSION

In this paper we have compared some of the important parameters of DRAM and MRAM technologies. As seen from the above table each memory technology has some advantages and disadvantages over the other technologies. It is not clear at this moment as which technology is more advantageous on the other or which is more reliable for design.
As mentioned earlier, it is difficult to compare the numbers of the table directly due to factors like difference in technology process, frequency, and architectural organization. For example MRAM cell being smaller than DRAM in actual usage they are larger than DRAM due to smaller fabrication process used in DRAM. The normalized power and the actual power also support this fact. But this is without the consideration of technology of fabrication and design used and hence the numbers are expected to vary much.

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